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In conventional semiconductor manufacture, a wafer which is well treated is cut into a plurality of chips, and fixed on a lead frame using gold (Au) wires to connect micro electrodes on the chip and pins of the lead frame. The above structure is then enclosed by suitable plastics to protect the internal semiconductor devices. The process to connect the chip to the lead frame and enclose the structure is referred to as packaging.

Page 1, line 17 to page 2, line 4, amend the paragraph as:

10-3  
The present advanced package, such as CSP (chip scale package), becomes much smaller, lighter, thinner, and shorter compared with the conventional package, such as QFP (Quad Flat Package) SOP (Small Outline Package) in order to reduce the cost. Meanwhile, ceramic packaging has been gradually replaced by plastic packaging. The reliability of the product is further enhanced by multi layer interconnect structure, protection layer process, and high quality of packaging. To further reduce the cost of packaging is greatly desired in the present IC industry. Therefore, advanced packaging such as CSP or wafer level CSP has been developed to increase the package density. MCM package is one of most promising techniques.

Page 2, lines 5-8, amend the paragraph as:

10-4  
KGD is defined as a chip that meets the specification and passes the test without wiring. To increase the qualified ratio of a MCM package in the semiconductor process, it is desired to use KGD in packaging. However, the use of KGD increases the cost of packaging.

Page 2, lines 11-16, amend the paragraph as:

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To overcome the above shortcoming in the conventional IC packaging, an object of the present invention is to provide a method of packaging MCM with CSPs as small and thin package bodies and integrating those bare chips and CSP into a ball grid array package (BGA package) to greatly reduce the cost because CSP test has advantages of easy test and low cost compared with conventional KGD test.

Page 2, lines 17-20, amend the paragraph as:

Another object of the present invention is to provide a MCM package structure of low cost and high reliability, which includes a substrate, one or more chip packages, a plurality of electrical connect pins, and a package material to enclose the substrate, the chips, and the chip package.

Page 4, line 10 to page 5, line 2, amend the paragraph as:

FIGs. 1A and 1B show the structure of a MCM package in the prior arts. The package body encloses a plurality of chips, which are interconnected by wire bonding or flip chip bonding. FIG. 1A schematically illustrates the package structure with wire bonding, which comprises a substrate 11, a plurality of chips 12, solder balls 13 under the substrate 11, wires 15 to connect the upper chip 121 and the substrate 11, and package mold resin 14. FIG. 1B schematically illustrates the package structure with flip chip bonding, which comprises a substrate 11, a plurality of chips 12, solder balls 13 under the substrate 11, ball bumps 16 to connect the lower chip 122 and the substrate 11, and package mold resin 14. Since the chips enclosed within the package are not examined by burn-in test and function test (F/T), the yield of the chips are not determined before

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packaging, and the yield of the package body after packaging can not be promoted. If four chips are enclosed within the package body and each chip has an average F/T yield 99%, the yield of the package is  $(99\%) \times (99\%) \times (99\%) \times (99\%) = 96\%$ .

Page 5, lines 3-6, amend the paragraph as:

Therefore, the F/T yield of the whole MCM package reduces to 96% after packaging the four chips. The more the chips packaged in the package, the less the yield. It is disadvantageous for the conventional MCM package to be used in advanced IC packaging in the future.

Page 5, lines 7-14, amend the paragraph as:

In the prior arts, one solution to overcoming the above disadvantage is to provide KGD. To prevent the F/T yield of the package from decreasing due to undetermined yield of the chips, both burn-in test and function test are needed for the chips, which will be packaged in subsequent packaging process. Those chips that pass through the above tests are called 'known-good dies', abbreviated as "KGDs". However, the KGD process imposes high cost because the size of the chip is very small and not easily fixed during burn-in test and function test.

Page 5, line 15 to page 6, line 6, amend the paragraph as:

The present invention provides an improved chip packaging method. FIGs. 2A-2D show CSP package structure in the prior arts. CSP is referred to the package that has a size just a little bigger than the chip and has a height less than 1.00 mm. FIG. 2A is a schematic diagram of CSP package structure with wire bonding in the prior arts, FIG. 2B

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is a schematic diagram of CSP package structure with flip chip bonding in the prior arts, FIG. 2C is a schematic diagram of another CSP package structure with a central pad bonding in the prior arts, and FIG. 2D is a schematic diagram of wafer level CSP in the prior arts. The CSP is not only light, thin, short, and small, but also passes through burn-in test and function test so that the yield of the CSP is not an issue. It is important that the cost of burn-in test and function test of CSP process is much lower than that of the KGD process. Another aspect is that CSP has no yield issue and can easily replace KGD process for integration into a MCM package because of light, thin, short, and small size.

Page 6, lines 7-11, amend the paragraph as:

Therefore, thin and small CSP or wafer level CSP after testing is served as KGD, which may include bare chips. Those bare chips can connect to the substrate by wire bonding or flip chip bonding, and the chips and CSP are further integrated into a ball grid array package (BGA package) so as to achieve the requirement of low cost and high quality for the MCM process.

Page 6, lines 14-20, amend the paragraph as:

FIG. 3A illustrates the first embodiment of MCM package structure in the present invention which includes CSP packages with wire bonding and flip chip bonding. The CSP is integrated into MCM package process, and includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP body 371 with wire bonding and is electrically connected to the substrate 31, and the CSP 372 with flip chip bonding is electrically connected to the substrate 31.

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Page 6, line 23 to page 7, line 5, amend the paragraph as:

FIG. 3B illustrates the second embodiment of MCM package structure in the present invention which includes CSP packages with flip chip bonding and central pad bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP 372 is electrically connected to the substrate 31, and the CSP 373 is electrically connected to the substrate 31 by the wire 35.

Page 7, lines 8-13, amend the paragraph as:

FIG. 3C illustrates the third embodiment of MCM package structure in the present invention which includes a bare chip and a CSP package with flip chip bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP body 372 is electrically connected to the substrate 31, and the bare chip 321 is electrically connected to the substrate 31 by the wire 35. FIG. 3D is a perspective view of the third embodiment of the MCM package structure in the present invention.

Page 7, lines 16-21, amend the paragraph as:

FIG. 3E illustrates the fourth embodiment of MCM package structure in the present invention which includes a bare chip and a CSP package with wire bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP body 371 is electrically connected to the substrate 31, and the bare chip 322 is electrically connected to the substrate 31 by means of flip-chip bonding.

Page 8, lines 1-7, amend the paragraph as: